Solution 5

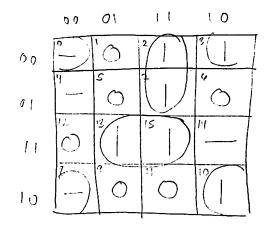
ECE Written Qualifying Examination, Spring 2019 Digital Logic

1. (5 points) Boolean Simplification.

Using K-maps, determine all the minimal sums for the following incomplete Boolean function.

$$f(w, x, y, z) = \sum m(2, 3, 7, 10, 13, 15) + dc(0, 4, 8, 14).$$

Recall that dc(0,4,8,14) means that the evaluation of f on the minterms m_0, m_4, m_8, m_{14} is undefined and should be chosen in such a way as to minimize the total cost.



2. (4 points) Boolean Algebra.

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Using Boolean Algebra postulates and theorems prove that

$$xy + x\overline{z} = (w + x + y)(\overline{x} + y + \overline{z})(w + x + \overline{y})(\overline{w} + x)$$

No credit will be given for solutions that use the truth table method.

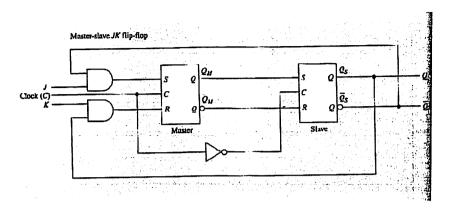
RHS =
$$(\omega + x + y)(\omega + x + \overline{g})(\overline{\omega} + x)(\overline{x} + y + \overline{z})$$

= $(\omega + x + (y \cdot \overline{y})](\overline{\omega} + x)(\overline{x} + y + \overline{z})$
= $(\omega + x + 0)(\overline{\omega} + x)(\overline{x} + y + \overline{z})$
= $(\omega + x)(\overline{\omega} + x)(\overline{x} + y + \overline{z})$
= $(x + 0)(\overline{x} + y + \overline{z})$

commutative distributive complement identity complement identity distributive complement identity

3. (6 points) Flip-Flops.

Recall the JK Master-Slave Flip-Flop pictured below.



(a) (3 points) Fill in the following function table, where Q^+ denotes the output Q in response to the inputs.

	Ing	mts	Outputs			
	K	С	Q+ Q+			
0	0		QQ			
0	1		01			
-1-	U	JĿ	10			
1	. 1		Q Q			
x	X	0	QQ			

(b) (3 points) Assume the control signal is 1, the slave latch is in its 1-state and a logic 0 is on both the J and K input lines. Then the K input line switches to logic 1 briefly and then back to logic 0. What happens to the slave state when the control signal returns to 0? Explain your answer.

Let S_{μ} , R_{μ} denote the input signals on the master latch and S_{μ} , R_{μ} denote the input signals on the slave latch. When K switches to logic 1, while S_{μ} remains at logic 0. So the master latch gets reset to 0. (i.e. $Q_{\mu} = 0$ and $Q_{\mu} = 1$). When K goes back to 0, R_{μ} switches to 0 so the moster latch remains in the 0 state (i.e. $Q_{\mu} = 0$ and $Q_{\mu} = 1$). Therefore, when the control signal inturns to 0, the challe of the slave latch goes to 0 (i.e. $Q_{\mu} = 0$ and $Q_{\mu} = 1$)

4. (5 points) State Diagram.

Draw the state diagram of a minimal Mealy machine having input line x, in which the signals $\{0,1\}$ are applied, and a single output line y. For $i=1,2,3,4,\ldots$ let x_i denote the i-th input values. For $i \in \{-2,-1,0\}$ let $x_i := 0$. For $i \geq 1$, the system is to produce an output of 1 coincident with input symbol x_i if the binary number represented by $(x_{i-3},x_{i-2},x_{i-1},x_i)$ is greater than or equal to 8 and 0 otherwise (where x_{i-3} is the most significant bit and x_i is the least significant bit.

An example of input/output sequences that satisfy the conditions of the system specification is:

i	1	2	3	4	5	6	7	8	9	10	11
\boldsymbol{x}	1	0	1	1	1	0	1	0	1	1	0
y	0	0	0	1	0	1	1	1	0	1	0

In the example above, the system produces an output of 1 coincident with the 4-th input symbol. This occurs since the 1-st, 2-nd, 3-rd and 4-th input symbols are 1,0,1,1, which represents the decimal number 11. Since $11 \ge 8$, the system outputs 1.

Your state diagram should have the minimum number of states possible.

