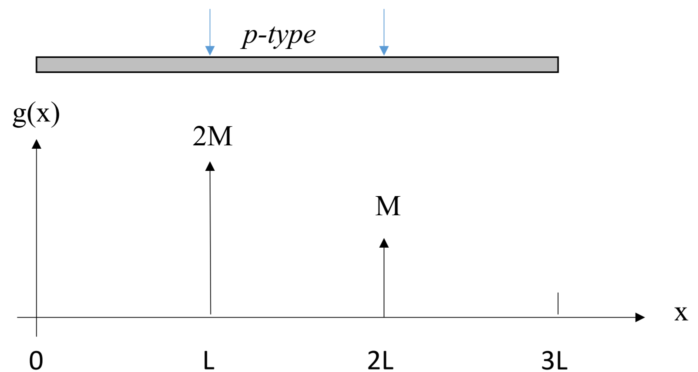
Devices – Spring 2019 Written Qualifying Examination

Problem 1 – Carrier Diffusion in 1-D

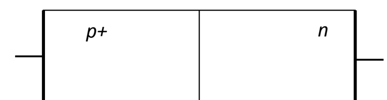


Consider the *one-dimensional* problem of a narrow, uniformly-doped, p-type bar of silicon of length 3L. Electron-hole pairs are being generated by light projected at two different locations. Light at x=L generates electron-hole pairs at a *rate* of g(L) = 2M and light at x=2L generates electron-hole pairs at a *rate* of g(2L) = M.

The minority carrier diffusion length constant Le is comparable to L. Assume that you know the doping concentration of the p-type silicon (N_A).

a) (2.5 pts) If we consider **the light source at x = L (with the light at x = 2L off)**, make a LARGE sketch of the minority carrier concentration *n(x)* from x = 0 to x = 3L. Be extremely clear about what the boundary conditions look like.
b) (2.5 pts) If we consider **ONLY the light source at x = 2L (with the light at x = L off)**, make a LARGE sketch of the minority carrier concentration *n(x)* from x = 0 to x = 3L. Be extremely clear about what the boundary conditions look like.
c) (2 pts) If we now consider **both light sources together**, make a LARGE sketch of the minority carrier concentration *n(x)* from x = 0 to x = 3L. Be extremely clear about what the boundary conditions look like.

Problem 2 – PN-junction diode



Consider a p^+-n diode with a highly doped p-side (concentration N_A) of length L and a lightly doped n-side (concentration N_D) of length L. Assume that L >> L_e and L >> L_h, the diffusion length of recombination of the minority carriers.

a) (4 pts) Make a LARGE, neat drawing of the minority carrier concentration that spans the whole length of the diode for forward-bias. Be sure to label the background minority carrier concentration level and the concentrations at the edges of the depletion region. Be sure to clearly indicate the shapes of the concentration plots (e.g., linear or curved)
b) (3 pts) Explain why the diode current is carried mostly by mobile holes.

Problem 3 – N-Channel Enhancement-Mode MOSFET

The standard formula for the above-threshold, saturation-mode, drain current in the nFET is: $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$

where V_{GS} is the gate to source voltage, V_t is the threshold voltage, k_n' is the process transconductance, and W/L is the width to length ratio. In the triode mode of operation, the drain current equation is given as:

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

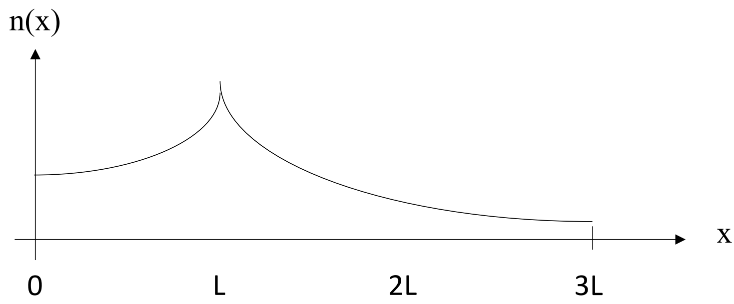
a) (3 pts) If the gate and drain are connected together, we have the “diode configuration”. Let’s imagine that the source is tied to ground (0 volts). If a current is known to be flowing into the drain, what is the voltage *difference* between the drain and the very end of the conducting *channel* on the drain-side? As the drain voltage is increased, how does this change (or not change)?

b) (3 pts) The body effect in an nFET is the change in the threshold voltage as a function of V_{SB}, the source to bulk voltage. $V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$ where γ is a parameter related to oxide capacitance and $2\phi_f$ is the surface potential for inversion. Provide a short explanation of why the threshold changes.

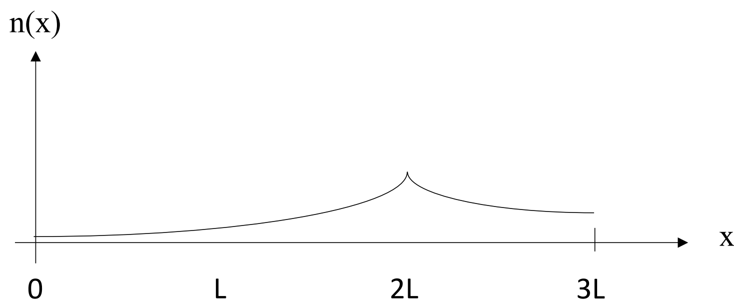
SOLUTIONS

Problem 1 – Carrier Diffusion in 1-D

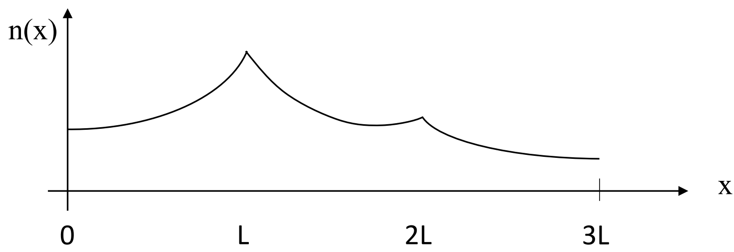
1a)



1b)

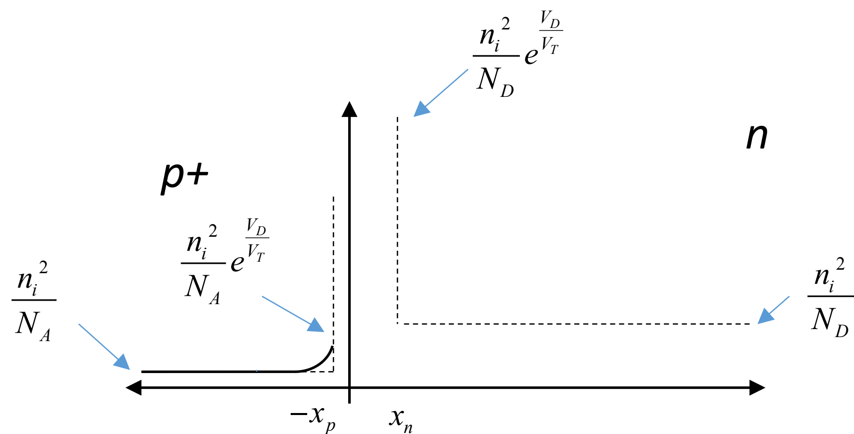


1c)



Problem 2 – p+-n diode

2a)



2b) The diode current is carried by both electrons moving from the n-side to the p-side and holes moving from the p-side to the n-side. The concentration of mobile electrons at the edge of the depletion region on the p-side is:

$n(-x_p) = \frac{n_i^2}{N_A} n_{p0} e^{\frac{V_D}{V_T}}$ and the concentration of mobile holes at the edge of the depletion region on the n-side is:

$p(x_n) = \frac{n_i^2}{N_D} p_{n0} e^{\frac{V_D}{V_T}}$ Because $N_A \gg N_D$, $n(-x_p) \ll p(x_n)$ This higher concentration of the mobile holes on the n-side leads to a higher hole current compared to the electron current.

The current density for electrons and holes is determined by the derivative of the minority carrier concentration plots at the depletion region edge and is proportional to $\frac{1}{N_A L_e}$ on the p-side and $\frac{1}{N_D L_h}$ on the n-side. (Note: the length constants decrease sublinearly with doping concentration)

Problem #3

3a) In the diode configuration, we know that we are in saturation because $V_{GS} = V_{DS} > V_{GS} - V_t$, provided that there is some positive drain current. In the saturated nFET, the voltage at the drain-end of the channel and highest voltage in the channel is $V_{GS} - V_t$. Therefore the voltage difference between drain and the end of the channel is $V_{GS} - (V_{GS} - V_t) = V_t$ Increasing the drain/gate voltage does not change this value.

3b) When the source voltage is raised above the body voltage $(V_{SB} > 0)$, the surface potential under the gate must rise up to V_{SB} for the channel between source and drain can be sustained. Because of the capacitor divider created by the gate oxide capacitance (Cox) and the depletion capacitance to the body, the gate voltage must be larger by more than V_{SB} for the surface potential to sit at V_{SB}. Thus, the required V_{GS} to form the channel is larger.